is proportional to a square of a ratio of the second resistance and the first resistance, said first and second resistances having a same type technology; and

a third resistance connected to said voltage ramp generator for generating a current ramp.

36. (Three Times Amended) A method for generating a ramp voltage comprising:

generating a capacitance charging current using an integrated circuit charging circuit produced using semiconductor technology and comprising a current generator having a first resistance and a circuit connected to the generator, the circuit having a second resistance and enabling the capacitance charging current to be proportional to a square of a ratio of the second resistance and the first resistance, said first and second resistances having a same type technology; and

charging a capacitance with the capacitance charging current for generating the ramp voltage.

37. (Twice Amended) A method according to Claim 36, wherein the circuit comprises a degenerate current mirror circuit.

REMARKS

Applicants would like to thank the Examiner for the thorough examination of the present application.

Independent Claims 9, 15, 21, 29 and 36 have been amended to more clearly define the present invention over the cited prior art references. These claims have been amended to recite that the integrated circuit voltage ramp generator and the integrated circuit current ramp generator are produced using semiconductor technology. Support may be found on page 4, lines 26-31 of the specification which provides that the components forming the voltage ramp generator and the current ramp generator are produced using CMOS technology or bipolar technology, for example. Certain dependent claims have been amended for consistency.

The independent claims have been further amended to highlight that the first and second resistances are of the same type of technology. Support may be found on page 7, lines 13-15 of the specification. The Applicants respectfully submit that the claims are supported by the specification. Attached hereto is a marked-up version of the changes made to the claims by the current amendment. The attached paper is captioned "Version With Markings to Show Changes Made."

The arguments and claim amendments supporting patentability of the claims are presented in detail below.

I. The Claims Are Patentable

The Examiner rejected independent Claims 9, 15, 21, 29 and 36 over the Applicants' prior art FIG. 1 in view of the Tanigawa patent and in view of the Lauffenburger patent. The Applicants' prior art FIG. 1 is directed to a current ramp generator. Tanigawa is directed to a gain control circuit of

the current mirror type, and Lauffenburger is directed to an apparatus and method for amplifying optically sensed signals.

The claimed invention, as recited in amended independent Claim 9, for example, is directed to an integrated circuit voltage ramp generator produced using semiconductor technology and comprising a capacitance and a charging circuit connected to the capacitance. The charging circuit comprises a current generator having a first resistance, and a circuit connected to the current generator and to the capacitance. The circuit has a second resistance, and enables a capacitance charging current to be proportional to a square of a ratio of the second resistance and the first resistance. In addition, independent Claim 9 further recites that the first and second resistances are of a same type technology.

Since the first and second resistances are of the same type technology, their respective spreads can be more easily compensated. This spread may be due to operating temperature changes, for example. As discussed on page 7, lines 11-24 of the specification, the second resistance may be chosen with a temperature variation coefficient of the same order of magnitude as that for the first resistance, for example. This advantageously allows compensation for variations in temperature due to the first resistance.

Without the second resistance, the spread of the first resistance may be reflected in variations of the capacitance charging current. To compensate for the spread of the first resistance, the second resistance is thus included. The capacitance charging current may also be controlled based upon the ratio of the second and first resistances. In

particular, the capacitance charging current is proportional to a square of a ratio of the second resistance and the first resistance, as recited in independent Claim 9.

Referring now more particularly to the Applicants' prior art FIG. 1, a ramp generator having a current source **Ig1** with no expressed teaching of the structure thereof is disclosed. The Examiner cited Tanigawa as disclosing in FIG. 4 a current sink comprising "a current mirror" which has the advantage of gain control.

The Examiner has taken the position that it would have been obvious to modify the current sink as disclosed in Tanigawa to a current source, and replace the current source **Ig1** in the Applicants' prior art FIG. 1 with the modified current source for obtaining a constant current with gain control. Moreover, the Examiner has further taken the position that since this modification yields a circuit identical in structure to the claimed invention, "it must inherently have the same function." The Applicants respectfully disagree based upon the following analysis.

In the Tanigawa patent, a gain control circuit of the current mirror type is disclosed in FIG. 4. The relationship between the signal current I_1 and the output current I_2 is based upon the equation $I_2 = I_1 * A$. The Examiner previously characterized the output current I_2 as the capacitance charging current in the present invention. The variable **A** is based upon the equation $\exp(V_{BE}/V_T)$, with V_T being a thermal voltage.

Referring to column 1, lines 59-61 in Tanigawa, which provides:

> "Therefore, the output current I_2 is set equal to a value A times larger than the input current I_1 ..." (Emphasis added.)

Tanigawa thus fails to teach or suggest that the capacitance charging current is proportional to a square of a ratio of the second resistance and the first resistance, as recited in independent Claim 9, for example.

The Examiner previously took the position that this argument only deals with the steady-state operation of the gain control device illustrated in FIG. 4 of Tanigawa. The Examiner further stated that this had nothing to do with the charging current that will exist when FIG. 4 is combined with the Applicants' prior art FIG. 1. However, in the discussion of FIG. 1 provided in the Background Section of the Applicants' specification, there is no reference that the capacitance charging current should be proportional to a square of a ratio of two different resistances, as recited in the Claimed 9.

Independent Claim 9 has also been amended to recite that the integrated circuit voltage ramp generator is produced using semiconductor technology, and that the first and second resistances are of the same type technology. Since the first and second resistances are of the same type technology, their respective spreads can be more readily compensated.

In semiconductor integrated circuits, components typically have broad spreads. With respect to the current ramp generator illustrated in the Applicants' prior art FIG. 1, the spreads of resistors **Rg1** and **Rs** induce large variations of the gradient **ΔIs/Δt**, as discussed on page 3, lines 5-14 in

the Applicants' specification. As discussed in the background section of the Applicants' specification, current ramp spreads are adjusted by adjusting the resistance **Rs** with memory points of the fuse type, as discussed on page 3, lines 15-24. This is a tedious and time consuming operation.

The second resistance in the claimed invention advantageously permits compensation for the variations of the first resistance. The gain control circuit illustrated in FIG. 4 of Tanigawa is a "conventional gain control circuit of the current mirror type." (column 1, lines 12-13). This gain control device is not suitable for semiconductor circuit integration. Reference is directed to column 1, line 65 through column 2, line 2 in Tanigawa, which provides:

> "However, since the variable resistor **R** is necessary to be connected to the emitter of the transistor **Q2** externally in the circuit shown in FIG. 4, an external leading terminal is required. Accordingly, the circuit of FIG. 4, as it is, is not suitable for semiconductor circuit integration." (Emphasis added.)

In other words, the resistance **R** in Tanigawa is not of the same type technology as the resistance **Rg1** in the Applicants' prior art FIG. 1. This is in sharp contrast to the claimed invention which recites that the first and second resistances have the same type technology. The Examiner cited Lauffenburger as disclosing circuitry being integrated onto a single substrate. The Applicants respectfully submit that Lauffenburger fails to provide the deficiencies as noted above, particularly with respect to the capacitance charging

current being proportional to a square of a ratio of the second resistance and the first resistance. In fact, Lauffenburger fails to even mention resistors or resistances with respect to generating a capacitance charging current.

Therefore, even if the references were combined as suggested by the Examiner, the claimed invention is not produced. In fact, Tanigawa teaches away from the claimed invention since the circuit illustrated in FIG. 4 is not suitable for semiconductor circuit integration (in particular, resistor **R**).

It thus appears that the Examiner is using impermissible hindsight reconstruction to modify Tanigawa in view of the Applicants' prior art FIG. 1 in an attempt to produce the claimed invention. The prior art references, individually or in combination, do not teach or suggest that 1) the first and second resistances having the same type of technology, and that 2) the capacitance charging current is proportional to a square of a ratio of the second resistance and the first resistance.

Accordingly, it is submitted that independent Claim 9 is patentable over the Applicants' prior art FIG. 1 in view of Tanigawa and Lauffenburger. Amended independent Claims 15, 21, 29 and 36 are similar to amended independent Claim 9. In view of the patentability of the independent claims as discussed above, it is submitted that their dependent claims, which recite yet further distinguishing features, are also patentable over the prior art. Thus, these dependent claims require no further discussion herein.

CONCLUSION

In view of the amendments to the claims and the arguments provided herein, it is submitted that all the claims are patentable. Accordingly, a Notice of Allowance is requested in due course. Should any minor informalities need to be addressed, the Examiner is encouraged to contact the undersigned attorney at the telephone number listed below.

Respectfully submitted,

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In re Patent Application of:
GARNIER ET AL.
Serial No. **09/499,060**
Filing Date: **February 4, 2000**

VERSION WITH MARKINGS TO SHOW CHANGES MADE

In the Claims:

The claims have been amended as follows:

9. (Three Times Amended) An integrated circuit voltage ramp generator produced using semiconductor technology and comprising:

[a semiconductor substrate;]

a capacitance [on said semiconductor substrate]; and

a charging circuit [on said semiconductor substrate and] connected to said capacitance and comprising

a current generator having a first resistance, and

a circuit connected to said current generator and to said capacitance, said circuit having a second resistance and enabling a capacitance charging current to be proportional to a square of a ratio of the second resistance and the first resistance, said first and second resistances having a same type technology.

15. (Three Times Amended) An integrated circuit voltage ramp generator produced using semiconductor technology and comprising:

[a semiconductor substrate;]

a capacitance [on said semiconductor substrate]; and

a charging circuit [on said semiconductor substrate and] connected to said capacitance and comprising

a current generator having a first resistance, and

a degenerate current mirror circuit connected to said current generator and to said capacitance, said degenerate current mirror circuit having a second resistance for generating a capacitance charging current that is proportional to a square of a ratio of the second resistance and the first resistance, said first and second resistances having a same type technology.

21. (Three Times Amended) An integrated circuit current ramp generator produced using semiconductor technology and comprising:

[a semiconductor substrate;]

a voltage ramp generator [on said semiconductor substrate and] comprising

a capacitance, and

a charging circuit connected to said capacitance and comprising

a current generator having a first resistance, and

a circuit connected to said current generator and to said capacitance, said circuit having a second resistance and enabling a capacitance charging current to be proportional to a square of a ratio of the second resistance and the first resistance, said first and second resistances having a same type technology; and

a conversion circuit [on said semiconductor substrate and] connected to said voltage ramp generator for generating a current ramp.

24. (Twice Amended) An integrated circuit current ramp generator according to Claim 21, wherein said charging circuit comprises a degenerate current mirror circuit [on said semiconductor substrate].

29. (Three Times Amended) An integrated circuit current ramp generator produced using semiconductor technology and comprising:

[a semiconductor substrate;]

a voltage ramp generator [on said semiconductor substrate and] comprising

a capacitance having a first resistance, and

a charging circuit connected to said capacitance and comprising

a current generator, and

a degenerate current mirror circuit connected to said current generator and to said capacitance, said degenerate current mirror circuit having a second resistance for generating a capacitance charging current that is proportional to a square of a ratio of the second resistance and the first resistance, said first and second resistances having a same type technology; and

a third resistance [on said semiconductor substrate and] connected to said voltage ramp generator for generating a current ramp.

36. (Three Times Amended) A method for generating a ramp voltage comprising:

generating a capacitance charging current using an integrated circuit charging circuit produced using semiconductor technology and comprising [a semiconductor substrate, and] a current generator [on the semiconductor substrate and] having a first resistance and a circuit [on the semiconductor substrate and] connected to the generator, the circuit having a second resistance [for] and enabling the capacitance charging current to be proportional to a square of a ratio of the second resistance and the first resistance, said first and second resistances having a same type technology; and

charging a capacitance [on the semiconductor substrate] with the capacitance charging current for generating the ramp voltage.

37. (Twice Amended) A method according to Claim 36, wherein the circuit comprises a degenerate current mirror circuit [on the semiconductor substrate].

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CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: DIRECTOR, U.S. PATENT AND TRADEMARK OFFICE, WASHINGTON, D.C. 20231, on this 24th day of October, 2002.